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COMPUTER AIDED DESIGN, DESIGN AUTOMATION AND LSI; KEYS TO HIGH---ETC(U)
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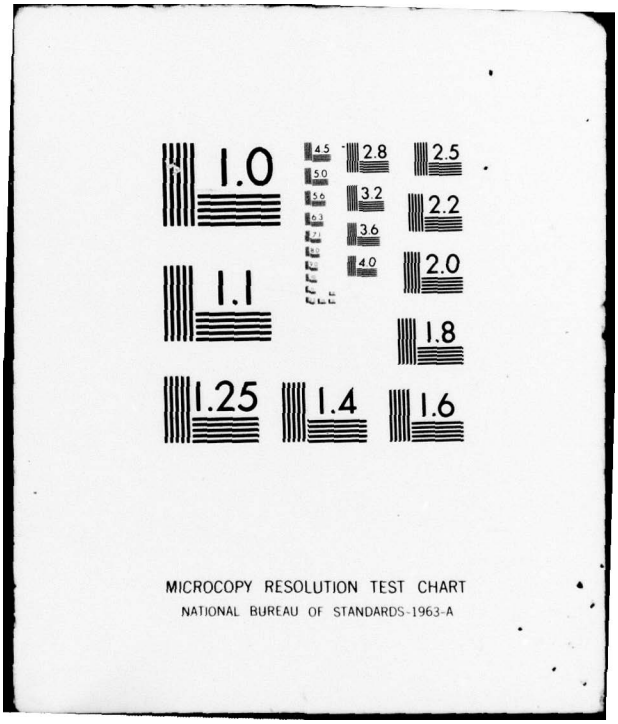
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(6) COMPUTER AIDED DESIGN, DESIGN AUTOMATION AND LSI; KEYS TO HIGH-PERFORMANCE MILITARY ELECTRONICS,

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INTRODUCTION

The Army is faced with the task of developing new and vastly improved electronic systems to meet the challenge of sophisticated, high-mobility, future battlefields. In general, this challenge requires the use of complex, custom, high-speed, low-power, large scale integrated circuits (LSICs) and very large scale integrated circuits (VLSICs). The successful development of such circuitry is dependent on the availability of advanced integrated circuit (IC) fabrication technologies, e.g., complementary metal oxide semiconductor/silicon on sapphire (CMOS/SOS) and gallium arsenide (GaAs) and on the availability of affordable design and design verification capabilities.

SHRINKING ARMY SYSTEMS/EQUIPMENT

The mobility of many Army systems is a function of their size and weight. Multiple-van, multiple-aircraft systems such as QUICKLOOK II-AGTELIS and CEFLY LANCER-TACELIS are examples where advanced IC technology could shrink the system and greatly enhance our ability to see and move on the battlefield.

Shrinking major Army systems requires high-speed, low-power, very complex integrated circuits at affordable cost. For example, current digital signal processors will require a twenty times reduction in size and weight, a five times or more reduction in power consumption and an increase of ten times to one hundred times in operating speed. Most important of all, the cost of developing the hardware must be reduced by at least ten times and turn-around time for custom IC

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development must be cut to three months.

ADVANCED ARMY SYSTEM IMPLEMENTATION

Advanced high-density, high-speed integrated circuit technologies are key ingredients for achieving the technical goals. The number of components in an integrated circuit has doubled every year for the past fifteen years. By 1980, chip complexities will be pushed to well beyond 100,000 components. ERADCOM programs in technologies such as CMOS/SOS, SOS, and GaAs will provide the high-speed (5 MHz-5 GHz) low-power performance characteristics needed for electronic counter-countermeasures (ECCM) data links and tactical signal intelligence (SIGINT). Such high-speed IC technology will allow the Army to implement very sophisticated, high-performance, extremely small electronic systems using both off-the-shelf integrated circuits (e.g., microprocessors and associated devices) and custom integrated circuits (e.g., random logic, microprocessors and "systems-on-a-chip").

CUSTOM LSI/VLSI....WHAT IS IT?

Today, the methods for developing custom LSI/VLSI devices fall into three categories:

(1) Handcrafted Approach....High volume (100,000 units) applications.

In the handcrafted design approach, the topological layout design is manually achieved with interactive graphic aids which are utilized extensively. Custom circuits are handcrafted when very large quantities of a device are required. This approach, which focuses on saving silicon area in favor of low initial design cost and turn-around time, is primarily utilized throughout the commercial semiconductor industry. The popular Intel 8080 and Motorola 6800 Microprocessors and random access memory devices are typical examples of handcrafted functions.

(2) Standard Cell Approach....Low to medium (1-100,000 units) quantity applications.

The standard cell approach emphasizes low initial design cost and quick turn-around. It is an automated capability that utilizes a library of design-optimized and performance-proven handcrafted standard logic cells and a placement and routing computer program that automatically generates complete LSI/VLSI topological layouts.

Although standard cell layouts are typically 10 to 20% larger than equivalent handcrafted functions, their design costs and turn-around time (not including processing time) can be from 25% to 40% of a handcrafted approach. The probability of standard cell LSI devices functioning properly the first time is five to ten times greater than for handcrafted designs.

(3) Universal Array Approach....Very low volume (1-1000 units) applications.

The universal array (UA) approach offers the lowest cost and quickest turn-around capability. It is well suited for very low volume applications such as prototyping, feasibility demonstration, and situations where low gate-count (100-300 gates)* is acceptable. UAs are prefabricated circuits comprising alternate rows of transistors for logic, and open areas for aluminum interconnection and feedthrus. All mask levels are defined except the metal mask level. The metal mask level is used to join individual transistors in order to form logic gates as well as to interconnect gates to form complete circuit functions. Topological layout design is typically a manual-planning, interactive-graphics-aided digitizing and editing process. Despite the advantages of fast fabrication cycles using stockpiled UAs, the manual generation and verification of UA layouts, the relatively low gate-count and the general unavailability of UAs, limit their acceptability and ultimate use. This situation will be vastly improved with the planned ERADCOM development of a new high gate-count (500-600 gates) universal array that is designed for optimum compatibility with automatic placement and routing and design verification programs.

CUSTOM LSI & CAD....A MARRIAGE OF TECHNOLOGIES

By the late 1960's, digital logic became the favored approach (over analog circuits) for implementing electronics in military systems. With the advent of the general-purpose digital microprocessor technology, this trend has continued. When off-the-shelf components have not been suitable to satisfy system size, weight, speed or power consumption requirements, then custom LSI has been considered.

*In this paper a gate is equivalent to four transistors.

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There have always been many questions concerning custom LSI availability. For example: Will the LSI circuit development cycle meet equipment/system schedules? How much will it cost? Who will fabricate and supply the devices? An early 1970 Electronics Command market survey discovered that custom LSI/VLSI circuits could not, in general, be obtained from large volume-oriented semiconductor vendors. These vendors were, and still are, focused on calculators, watches, games, microprocessors, memories and automotive circuits. It was determined that custom LSI would have to come from the people who build military systems; namely, defense systems contractors. Many of the defense systems contractors that were surveyed were not prepared to develop LSI because of their lack of qualified design personnel, design tools and IC fabrication facilities. For the few vendors who could provide custom LSI for low volume applications, it was determined that relatively simple LSI devices would require at least a one-year, $100K development cycle, For major systems, wherein several custom circuits were required, it became obvious that conventional manual design approaches could not meet system schedules and cost requirements. Clearly, the defense systems industry required an automated design approach to remedy this situation.

EARLY CAD....

Early design automation approaches for custom LSI were evaluated against Army requirements for high-density, high-speed, low-power circuitry. National Aeronautics and Space Administration (NASA) sponsored CAD, based on the utilization of a family of single-side entry, bulk-silicon CMOS standard cells and an automatic placement and routing program called PR2D, was of particular interest. Evaluation of this approach indicated that PR2D-generated LSI topological layouts were about five to ten times larger than handcrafted equivalents. The layouts were large because: (1) the metal gate bulk CMOS standard cells developed for PR2D use were large; (2) the placement and routing algorithms forced a hugh build-up of interconnection metalization on the sides of chips while the areas between cell rows was wasted. The most serious drawback was the speed limitation imposed by the parasitic capacitance and resistance that is inherent with the excessive interconnect metalization. Since the PR2D approach could not provide sufficient high-density, high-speed chip layouts for future Army battlefield requirements, a new approach had to be developed.

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MP2D....A BREAKTHRU FOR CUSTOM LSI

New concepts in automated LSI design based on the utilization of double-entry standard cells, feedthru cells and new and improved placement and routing algorithms, have resulted in a new area-efficient, cost-effective and multi-technology useful layout program called MP2D. MP2D is a significant improvement over the early 1970 vintage PR2D program as it provides for a 4:1 reduction in chip area. For example, the 250 gate (1000 transistor) LSI circuit in Figure 1 is 50,284 sq mils using PR2D and 11,700 sq mils with MP2D.

The application of MP2D is based on the placement of box outlines of logic cells which describe the physical size and input/output connections to standard cells, and the interconnection of the cells as prescribed by a user supplied net list. MP2D can, therefore, be utilized for any IC technology that can provide double-entry cells and a two-level interconnection scheme. For this reason, MP2D is utilized for applications that involve the use of CMOS/SOS and radiation-hardened CMOS/SOS, C^2L, I^2L and universal array technologies.

MP2D is also challenging the handcrafted layout approach for higher volume applications. The computer charges for generating the high density layout in Figure 1 was $230 for 30 CPU minutes on an IBM 360/65. Although a handcrafted equivalent of the same function might be 10-20% smaller in area, it is estimated that about 6 to 8 manweeks would be required to manually generate, verify, edit and digitize a handcrafted layout. Should customer requirements change, a new layout via design automation requires only another 30 minute computer run; a manual redesign would require days or weeks, depending on the extent of the changes.

For a custom LSI circuit to be cost-and-time-affordable in military systems, it is critical that the circuit go through only a single very rapid design, fabrication and testing cycle; the chip has to work the first time. The rapid, low-cost development of an LSI chip, therefore, requires more than the automated layout program MP2D. Since the circuit designer cannot realistically breadboard a custom function, fast computer logic simulation is also required. Testing a custom LSI part also requires computer generated test patterns. This means that logic/circuit designers require a total CAD system that can automate all phases of custom LSI design.

ARMY CADDA CENTER FOR CUSTOM LSI

The Electronics Technology and Devices Laboratory, ERADCOM, Fort Monmouth, New Jersey has established an Army computer-aided design and design-automation (CADDA) center for affordable custom LSI. An extensive system of CADDA programs (Figure 2), standard cells and an interactive graphics facility have been developed and implemented during the past several years by ET&DL.

MP2D has been built into the CADDA system which includes a logic simulation program, LOGSIM; a test pattern generation program. AGAT; a common data base system, CDB; and an interface to an Applicon interactive graphic system. In addition, a family of 40, MP2D-compatible, high-density, double-entry CMOS/SOS standard cells was designed, verified and documented. To generate LSI devices using this capability, the designer partitions his logic into standard cells, provides a net list containing cell pattern numbers and their connectivity, and enters the CADDA system via the common data base. Having entered CDB, the designer selects and executes the design programs via control cards. The topological output of the design system is a magnetic tape data file that is loaded into the Applicon interactive graphic system. Once the file is loaded into the Applicon, the LSI/VLSI layout can be edited or modified, for example, to reduce the delay of critical paths, to optimize performance or to relocate or re-orient bonding pads. CALCOMP plots for error checking and general documentation and magnetic tape files for photomask making are also accomplished with the Applicon system.

CADDA TECHNICAL IMPACT

The return on the Army's investment in the advanced CADDA system is in the utilization of the software, standard cells and system-user techniques which are offered to technical groups with a clear U. S. military objective. ERADCOM's ET&D Laboratory has formed a CADDA User's group comprising a continually increasing number of defense systems contractors and other government agencies (Figure 3) who are using the automated LSI/VLSI design software, cells, etc. The use of the Army CADDA software and standard cells is committed to at least six major military programs, such as PATRIOT, REMBASS and PLRS, and is being considered for use in many other systems.

A custom LSI fuze circuit for the PATRIOT missile is a good example of the impact that custom LSI and CAD can have (Figure 4). The one-chip CMOS/SOS circuit provided significant reductions in size,

power consumption, and cost compared to an equivalent TTL implementation. The LSI circuit which contains over 2000 devices was topologically layed out by MP2D at a cost of less than $400.

NEW CADDA FOR THE FUTURE

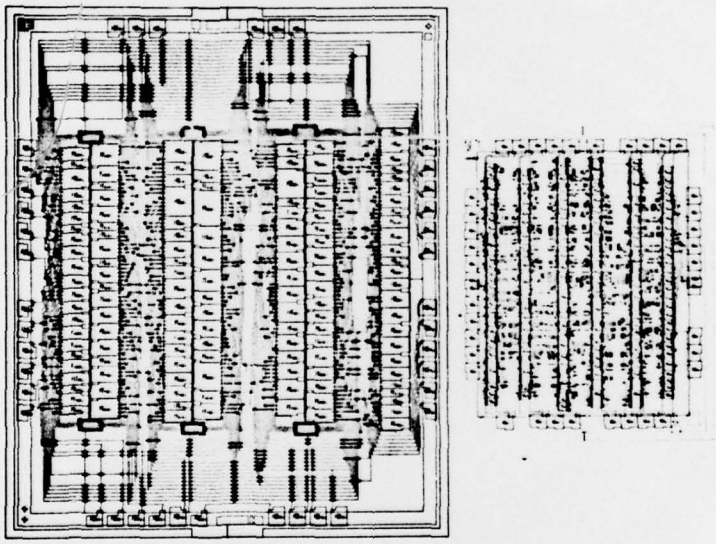
The trend for Army integrated electronics is toward significantly higher speeds and circuit complexities. Higher operating speed is a function of the speed of the active devices within the standard cells and of the parasitic impedances of the chip interconnections. In the next couple of years, by improving the CMOS/SOS technology and reducing the SOS device channel length, standard cells will operate at frequencies in excess of 200 MHz. Parasitic interconnect impedances will be minimized by improved CMOS/SOS processing and by reducing the physical length of electrical connections. The MP2D program is presently being modified to automatically minimize user-identified critical networks (paths). The program will: control the length of each wire segment, compute and print out actual RC data, and tell the designer if a specified delay limit is exceeded. "System-on-a-chip" custom arrays of VLSI complexity will be accomplished by incorporating, within MP2D, the capability to mix high-density, high-speed, hand-crafted supercells with standard cells. Circuit densities with figures-of-merit below 10 sq mils/device will be achieved using this approach. Linear and digital functions will also be customized together using the supercell MP2D approach.

SUMMARY

A deterrent to the utilization of custom LSI functions has been the lack of an automated design and development system that will allow rapid development of circuits in a single, cost-effective cycle. The manual design of LSI circuits in one year, $100K cycles is too costly for low volume military applications.

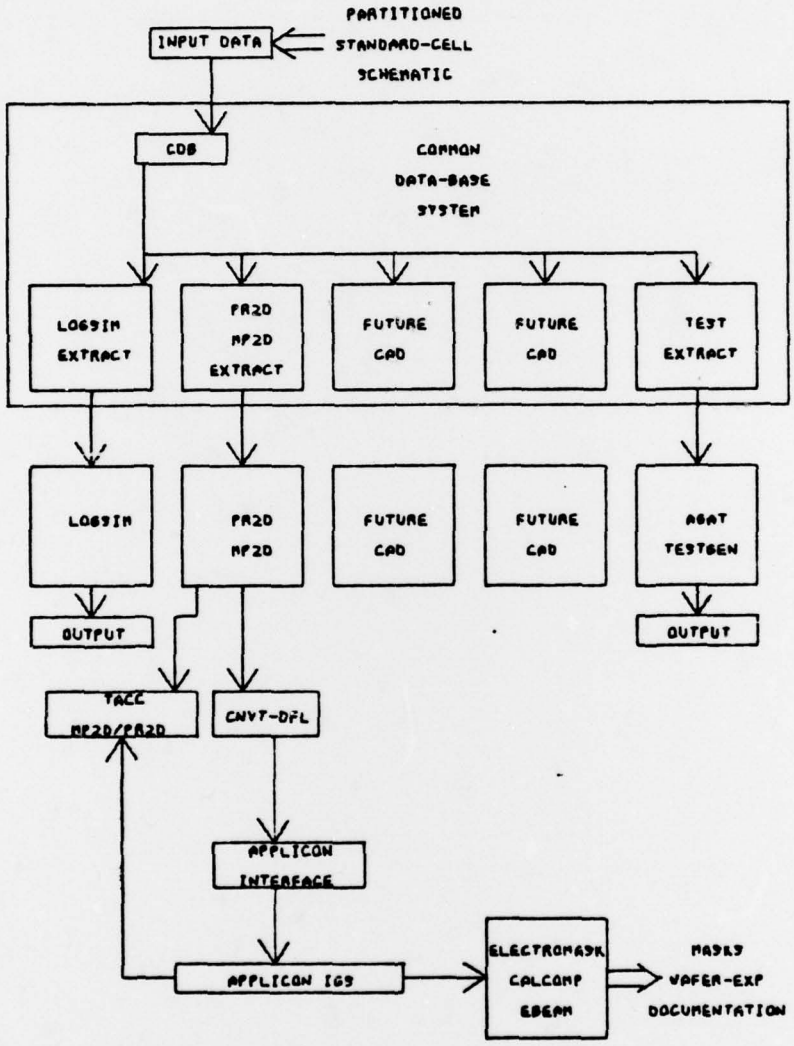
ERADCOM's Electronics Technology & Devices Laboratory, Fort Monmouth, N. J., has developed a complete CADDA system for custom LSI that make feasible three-month $35K development cycles. The system is applicable to a wide variety of advanced IC technologies such as CMOS/SOS, radiation-hardened CMOS/SOS, bulk CMOS I^2L and universal arrays.

Key elements of the CADDA system have been widely disseminated to defense systems contractors and are being applied to major Army equipment. Major enhancements are underway to extend the availability of custom LSI to much higher frequencies and levels of complexity.



ERADCOM MP2D LAYOUT PROGRAM REDUCES STANDARD CELL LAYOUTS BY 4:1
COMPARED TO PR2D PROGRAM

Figure 1



ERADCOM CADDA SYSTEM FOR CUSTOM LSI

Figure 2

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RCA CORPORATION	CAMDEN, SOMERVILLE, NEW JERSEY
RAYTHEON COMPANY	BEDFORD, MASSACHUSETTS
E-SYSTEMS	ST. PETERSBURG, FLORIDA
McDONNELL DOUGLAS	MONROVIA, CALIFORNIA
TRW SYSTEMS	REDONDO BEACH, CALIFORNIA
HARRIS ELECTRONIC SYSTEMS DIVISION	MELBOURNE, FLORIDA
BENDIX CORPORATION	BALTIMORE, MARYLAND
MAGNAVOX CORPORATION	FORT WAYNE, INDIANA
HUGHES AIRCRAFT COMPANY	LOS ANGELES, CALIFORNIA
ROCKWELL INTERNATIONAL	NEWPORT BEACH, CALIFORNIA
SOLID STATE SCIENTIFIC	MONTGOMERYVILLE, PENNSYLVANIA
SPERRY UNIVAC	ST PAUL, MINNESOTA
ITT SEMICONDUCTORS	WEST PALM BEACH, FLORIDA
SANDIA LABORATORIES	ALBUQUERQUE, NEW MEXICO
NASA	HUNTSVILLE, ALABAMA
NAFI	INDIANAPOLIS, INDIANA

USERS OF ERADCOM CADDA PROGRAMS

Figure 3

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	IC VERSION	LSI(ERADCOM MP2D LAYOUT)
Technology	TTL	SOS/CMOS
Packages	31	1
External Parts	9	8
Power Consumed	4.5W	1.2 mW
Relative Cost	10	1

IMPACT OF LSI & CAD ON SYSTEM COST/PERFORMANCE
FOR FUZE LOGIC, PATRIOT MISSILE

Figure 4

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